EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Tom Brennan (Reg. No. 35,075) on 11/18/2008.

The application has been amended as follows:

The title has been amended to "System and Method for Processing Memory Instructions Using a Forced Order Queue."

The claims have been amended as follows:

7. A computerized method for accessing data in a memory system having a local cache and a higher level cache, comprising:

obtaining a memory request;

storing the memory request in an Initial Request Queue (IRQ); and

processing the memory request from the IRQ by a cache controller, wherein processing includes:

determining whether the memory request hits in the local cache;

determining whether a portion of an address associated with the memory request matches one or more partial addresses in a Force Order Queue (FOQ), wherein the FOQ stores a memory request that is pending to the higher level cache;

when the portion of an address associated with the memory request does not match the one or more partial addresses in the FOQ and, at the same time, the

memory request hits in the local cache, servicing the memory request immediately using data in the local cache without adding the memory request to the FOQ;

when the portion of an address associated with the memory request does not match the one or more partial addresses in the FOQ and, at the same time, the memory request misses in the local cache, adding the memory request to the FOQ, allocating a cache line in the local cache corresponding to the local cache miss and servicing the memory request using data received from the higher level cache;

when the portion of an address associated with the memory request matches the one or more partial addresses in the FOQ and, at the same time, the memory request hits in the local cache, preventing the memory request from being satisfied in the local cache, wherein preventing includes adding the memory request to the FOQ and servicing the memory request using data received from the higher level cache; and

when the portion of an address associated with the memory request matches the one or more partial addresses in the FOQ and, at the same time, the memory request misses in the local cache, preventing the memory request from being satisfied in the local cache, wherein preventing includes adding the memory request to the FOQ and servicing the memory request using data received from the higher level cache.

22. A scalar processor, comprising:

a local cache;

an Initial Request Queue (IRQ); and

a cache controller having a Force Order Queue (FOQ), wherein the FOQ stores a scalar memory request that missed in the local cache and is pending to a higher level cache;

wherein the IRQ buffers a scalar load/store memory request having a scalar load/store instruction and its one or more associated addresses and sends the scalar load/store memory request to the cache controller and the local cache;

wherein, when a portion of the one or more associated addresses of the scalar load/store memory request does not match one or more partial addresses in the FOQ and, at the same time, the scalar load/store memory request hits in the local cache, the local cache services the scalar load/store memory request received from the IRQ without adding the memory request to the FOQ;

wherein, when the portion of the one or more associated addresses of the scalar load/store memory request does not match the one or more partial addressed in the FOQ and, at the same time, the scalar load/store memory request misses in the local cache, the scalar load/store memory request is added to the FOQ, one or more lines in the local cache are allocated for cache line replacement, and the scalar load/store memory request is passed to the higher level cache;

wherein, when the portion of the one or more associated addresses of the scalar load/store memory request matches the one or more partial addresses in the FOQ and, at the same time, the scalar load/store memory request hits in the local cache, the scalar load/store memory request is added to the FOQ and the scalar load/store memory request is passed to the higher level cache; and

wherein, when the portion of the one or more associated addresses of the scalar load/store memory request matches the one or more partial addresses in the FOQ and, at the same time, the scalar load/store memory request misses in the local cache, the scalar load/store memory request is added to the FOQ and the scalar load/store memory request is passed to the higher level cache.

29. (Currently Amended) A scalar processor, comprising:

a local cache;

an Initial Request Queue (IRQ); and

a plurality of cache controllers, wherein each cache controller includes a Force Order Queue (FOQ), wherein the cache controllers receive scalar memory requests from the IRQ and wherein, when a cache controller receives such a scalar memory request, the cache controller stores the scalar memory request in its FOQ if the scalar memory request misses in the local cache and is pending to a higher level cache;

wherein the IRQ buffers a scalar load/store memory request having a scalar load/store instruction and its one or more associated addresses and sends the scalar load/store memory request to the local cache and to one of the plurality of cache controllers corresponding to the one or more associated addresses of the scalar load/store memory request;

wherein, when a portion of the one or more associated addresses of the scalar load/store memory request does not match one or more partial addresses in the FOQ and, at the same time, the scalar load/store memory request hits in the local cache, the local cache services the scalar load/store memory request received from the IRQ without adding the memory request to the FOQ;

wherein, when the portion of the one or more associated addresses of the scalar load/store memory request does not match the one or more partial addressed in the FOQ and, at the same time, the scalar load/store memory request misses in the local cache, the scalar load/store memory request is added to the FOQ, one or more lines in the local cache are allocated for cache line replacement, and the scalar load/store memory request is passed to the higher level cache;

wherein, when the portion of the one or more associated addresses of the scalar load/store memory request matches the one or more partial addresses in the FOQ and, at the same time, the scalar load/store memory request hits in the local cache, the scalar load/store command is added to the FOQ and the scalar load/store memory request is passed to the higher level cache; and

wherein, when the portion of the one or more associated addresses of the scalar load/store memory request matches the one or more partial addresses in the FOQ and, at the same time, the scalar load/store memory request misses in the local cache, the scalar load/store memory request is added to the FOQ and the scalar load/store memory request is passed to the higher level cache.

Claim 33 has been added.

33. The computerized method of claim 7, wherein the FOQ is divided logically into a first and second queue, wherein the first queue monitors scalar memory requests to the higher level cache and the second queue monitors scalar memory requests that are serviced by the higher level cache but not yet written to the local cache.

Claims 1-6, 16-21, 26-28 have been CANCELED.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

Claims 7,8,14,15,22,24,25, and 29-33 (renumbered 1-12) are allowable over the prior art of record.

Applicant's amendment to the claims filed 10/30/2008 resulted in an updated search by the Examiner and the finding of the prior art of Frederick, Jr.; the Examiner initiated an interview on 11/18/2008 to present the prior art reference of Frederick, Jr. The Examiner conceded that Applicant's amended claims on 10/30/2008 clearly distinguished the previous §103 rejection for claim 7. However, the Examiner stated in the interview that if the Miss Address Buffer of Hughes was considered as teaching Applicant's Forced Order Queue, then Hughes would teach the amendment limitation of "… servicing the memory request immediately using data in the local cache without adding the memory request to the FOQ." It would follow that Hughes' Miss Address Buffer would then not teach the last limitation of claim 7, but the prior art of Fredrick could be cited in the rejection in order to teach an incoming address matches an address in the FOQ, preventing the request from being satisfied in the cache, including adding the request to the FOQ (step 310, figure 3).

Applicant proposed a second amendment to the claims to overcome the newly cited art of Frederick, JR. and resulted in the claims as presented by the Examiner's amendment above.

Applicant's arguments filed 10/30/2008 in regards to claims 31 and 32 are persuasive and the §112, first paragraph, rejection has been withdrawn by the Examiner hereto.

As per claims 7, 22, and 29, the prior art of record does not teach or suggest, either alone or in combination, the entirety of limitations of the claims. Specifically, the prior art does not teach each of the claimed interactions with the FOQ and the local memory.

Claims 8,14,15,24,25, and 30-33 are allowable as being dependent upon an allowable base claim.

Collins et al., "Hardware Identification of Cache Conflict Misses," teaches an Adaptive Miss Buffer but does not specifically teach a Forced Order Queue that operates with a caching system as claimed by the Applicant.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHANE M. THOMAS whose telephone number is (571)272-4188. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shane M Thomas/ 24 November 2008
Patent Examiner, Art Unit 2186